

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

A22 1 1. (Currently Amended) A digital processing system having a
2 microprocessor, wherein the microprocessor comprises:
3 fetch circuitry for fetching instruction fetch packets from
4 sequential memory address locations, wherein each fetch packet
5 contains a first plurality of instructions, each instruction
6 including an instruction type and a predetermined p-bit, said p-bit
7 having a first digital state indicating a next instruction is to
8 execute in parallel with said instruction and a second digital
9 state indicating a next instruction is to execute in a cycle after
10 said instruction;
11 a second plurality of functional units, each of the second
12 plurality of functional units operable to execute a second
13 plurality of instructions corresponding instruction in parallel
14 with other functional units, and
15 dispatch circuitry connected to said fetch circuitry and said
16 second plurality of functional units operable to
17 select an execution packet from one or more fetch
18 packets, wherein an execute packet varies in size and contains
19 only a set of instructions that can be executed in parallel on
20 the plurality of functional units, ~~whereby a first execute~~
21 ~~packet contains a different number of instructions than a~~
22 ~~second execute packet due to resource constraints by scanning~~
23 instructions from lower memory address locations to higher
24 memory address locations adding an instruction to said execute
25 packet when said p-bit of a prior instruction has said first
26 digital state until said p-bit of an instruction has said
27 second digital state, and

28 dispatch each instruction of said selected execute packet
29 to a functional unit corresponding to said instruction type of
30 said instruction.

1 2. (Original) The digital processing system of Claim 1,
2 wherein the first plurality is equal in number to the second
3 plurality.

Claim 3 (Cancelled)

1 4. (Currently Amended) The digital processing system of
2 Claim 3 2, wherein the dispatch circuitry comprises:

3 a first latch to hold ~~the~~ said first plurality of instructions
4 of a first fetch packet;

5 a second latch to hold ~~the~~ said first plurality of
6 instructions of a second fetch packet immediately following said
7 first fetch packet;

8 ~~selection circuitry to select a first portion of the first~~
9 ~~execute packet from the first latch and a second portion of the~~
10 ~~first execute packet from the second latch~~

11 a first plurality of multiplexers, each multiplexer having a
12 first input receiving an instruction from a predetermined position
13 of said first latch, a second input receiving an instruction from a
14 corresponding position of said second latch, a control input and an
15 output, each multiplexer selecting at said output said instruction
16 from said first latch, said instruction from said second latch or
17 no instruction dependent upon said control input;

18 a dispatch control circuit connected to said first latch, said
19 second latch and said plurality of multiplexers, said dispatch
20 control circuit receiving said predetermined p-bit from each
21 instruction of said first latch and each instruction of said second
22 latch for control of said plurality of multiplexers via said

23 control inputs according the execute packets determined by said p-
24 bits; and

A22
25 a cross point circuitry connected to said plurality of
26 multiplexers for dispatching said instructions at said output of
27 said multiplexers to a functional unit corresponding to said
28 instruction type of each instruction.

Claims 5 and 6 (Canceled)

1 7. (Currently Amended) A method of operating a digital
2 system having a microprocessor, wherein the microprocessor has a
3 plurality of functional units for executing instructions in
4 parallel, comprising the steps of:

5 storing instructions at sequential memory address locations,
6 each instruction including an instruction type and a predetermined
7 p-bit, said p-bit having a first digital state indicating a next
8 instruction is to execute in parallel with said instruction and a
9 second digital state indicating a next instruction is to execute in
10 a cycle after said instruction;

11 fetching a sequence of instruction fetch packets, wherein each
12 fetch packet contains a first plurality of instructions;

13 ~~examining~~ scanning the p-bit of each instruction of each fetch
14 packet from lowest memory address location to highest memory
15 address location to determine an execution execute packet boundary
16 dependent on the p-bits;

17 ~~selecting a first portion of an execute packet from a first~~
18 ~~fetch packet and a second portion of a first execute packet from a~~
19 ~~second fetch packet if the first execute packet boundaries span the~~
20 ~~first fetch packet and the second fetch packet~~

21 dispatching each instruction within the determined execute
22 packet to one of a second plurality of execution units dependent
23 upon an instruction type of the instruction.

1 8. (New) The method of Claim 7, wherein:
A222 2 the first plurality of instructions in a fetch packet equals
3 the second plurality of functional units.

1 9. (New) The method of Claim 7, wherein:
2 said step of determining an execute packet boundary dependent
3 upon the p-bits includes
4 storing a first fetch packet in a first latch,
5 storing a second fetch packet in a second latch,
6 selecting an instruction from said first latch, a
7 corresponding instruction from said second latch or no
8 instruction dependent upon said p-bit from each instruction of
9 said first latch and each instruction of said second latch.

1 10. (New) A digital processing system having a
2 microprocessor, wherein the microprocessor comprises:

3 fetch circuitry for fetching instruction fetch packets from
4 sequential memory address locations, wherein each fetch packet
5 contains a first plurality of instructions, each instruction
6 including an indication of a corresponding functional unit and an
7 indication of an execute packet;

8 a second plurality of functional units, each of the second
9 plurality of functional units operable to execute a corresponding
10 instruction in parallel with other functional units, and

11 dispatch circuitry connected to said fetch circuitry and said
12 second plurality of functional units operable to

13 select an execute packet from one or more fetch packets,
14 wherein an execute packet varies in size and contains only a
15 set of instructions that can be executed in parallel on the
16 plurality of functional units, by scanning instructions from
17 lower memory address locations to higher memory address

P22

18 locations adding an instruction to said execute packet
19 dependent upon said indication of an execute packet, wherein
20 upon a branch into the middle of an execute packet not
21 selecting instructions having memory address locations lower
22 than the branch, and
23 dispatching each instruction of said selected execute
24 packet to a corresponding functional unit.

1 11. (New) A method of operating a digital system having a
2 microprocessor, wherein the microprocessor has a plurality of
3 functional units for executing instructions in parallel, comprising
4 the steps of:
5 storing instructions at sequential memory address locations,
6 each instruction including an indication of a corresponding
7 functional unit and an indication of an execute packet;
8 fetching a sequence of a first plurality instruction fetch
9 packets, wherein each fetch packet contains a first plurality of
10 instructions;
11 scanning the indication of execute packet of each instruction
12 of each fetch packet from lowest memory address location to highest
13 memory address location to determine an execute packet, wherein
14 upon a branch into the middle of an execute packet not selecting
15 instructions having memory address locations lower than the branch;
16 dispatching each instruction within the determined execute
17 packet to a corresponding execution unit.